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**LETTER TO THE EDITOR**

# Differential negative resistance in a one-dimensional mesoscopic system due to single-electron tunnelling

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**Abstract.** We present studies in the DC voltage bias regime of a split-gate device utilising the high-mobility electron gas of a GaAs/AlGaAs heterojunction. We find oscillations in the *I–V* characteristic of a one-dimensional channel which we relate to single-electron tunnelling events in the channel. The effects are explained using a mesoscopic model possibly involving the presence of an impurity in the channel and the role of the device capacitance. The particular aspect of this system of importance is that unlike in conventional capacitors, the capacitance and resistance of depleted regions varies with the trapped charge.

The study of one-dimensional systems using GaAs/AlGaAs heterojunctions to confine the electrons to two dimensions, and then further confining the electrons to one dimension by means of a 'split-gate' Schottky barrier was initially introduced by Thornton *et al* [1]. One-dimensional ballistic transport has recently received much attention following the finding that if the channel in which the electrons are confined is sufficiently short that no scattering occurs as the electrons traverse the system, then a one-dimensional sub-band has a quantised resistance [2, 3]. If there are $i$ sub-bands in the system then the resistance, in the absence of a magnetic field, becomes $h/2e^2i$ and jumps between roughly quantised values when $i$ changes by one due to a change of width or Fermi energy. In this letter we present results taken using a particular split-gate device in the DC bias regime. For a fixed gate voltage we find that the current oscillates with source–drain voltage, an effect that we relate to single-electron tunnelling events occurring within the channel. We note that the maximum resistance of a 1D ballistic device corresponds to occupation of the ground sub-band only and has a value 12.6 kΩ. Consequently values of resistance greater than this indicate that tunnelling into the channel is determining the resistance.

The basis of the split-gate family of devices is the GaAs/AlGaAs heterojunction grown by molecular beam epitaxy, where the two-dimensional electron gas is confined at the GaAs/AlGaAs interface. The heterojunction wafer used here consisted of the following layers: a semi-insulating GaAs substrate on which is grown a superlattice buffer ((AlAs 2.5 nm, GaAs 2.5 nm) × 20), 1 μm nominally undoped GaAs, 20 nm

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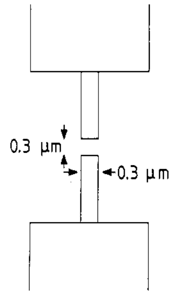


**Figure 1.** A schematic diagram of the gate pattern on the device used in the experiments.

undoped AlGaAs, 40 nm AlGaAs Si doped at $10^{18}$ cm$^{-3}$, followed by a 10 nm undoped GaAs capping layer.

The two-dimensional electron gas at the GaAs–$Al_{0.37}Ga_{0.63}As$ interface had a carrier concentration of $2.75 \times 10^{11}$ cm$^{-2}$ and an electron mobility of 98 m$^2$ V$^{-1}$ s$^{-1}$ both measured at 4.2 K in the dark. The Schottky barriers used to confine further electronic transport were defined by high-resolution electron beam lithography. The fabrication process consisted of five distinct stages. Initially 1500 Å of polymethylmethacrylate (PMMA) was spun onto the heterojunction surface and baked at a temperature greater than 100 °C. The required pattern was then exposed in the resist using an electron beam of extremely small diameter (i.e. less than 500 Å). After exposure the pattern was developed for approximately 30 s in a mixture of IPA/MIBK which leaves the required pattern exposed on the mesa previously fabricated by optical lithography techniques. The final stage consisted of evaporating 500 Å of gold onto the surface, the excess of which along with the remaining PMMA is then lifted off in acetone. The metallisation pattern with dimensions is illustrated in figure 1.

The behaviour of one-dimensional ballistic channels when DC current biased to high electrical fields has been studied previously [4, 5, 6]. These devices are in the mesoscopic regime; that is, they are sensitive to single impurities or defects giving rise to such phenomena as universal conductance fluctuations. Suitably placed impurities can give rise to scattering and various resonance phenomena in the transition from diffusive to ballistic propagation. Here we present a further mesoscopic effect in the presence of a high electric field. In the experiment the device was pinched off (i.e the electron gas between the gates was fully depleted) and then the conductance was induced by increasing the DC bias applied between the source and drain. Thus, the circuit was effectively voltage biased as discussed below. We note that a rough calculation of the capacitance indicates that we are in the regime where single-electron effects are of significance.

Figure 2 illustrates the results obtained at 4.2 K from a device that pinched off at a particularly low gate voltage (−0.4 V). The principal feature of the results is the oscillation in current as a function of source–drain voltage, the periodicity of which varies as the width of the channel is varied by varying the gate voltage. The oscillations are not dissimilar to the current steps predicted for two ultra-small capacitors in series [7], except that the current shows abrupt periodic decreases rather than increases. A complete description of the single-electron transport process requires a quantum treatment [8, 9, 10]. However, in the case described here we are considering hot, non-degenerate electrons with a very short phase coherence length. Consequently, we base our discussion on semi-classical considerations. We feel that this is justified as, depending on the device

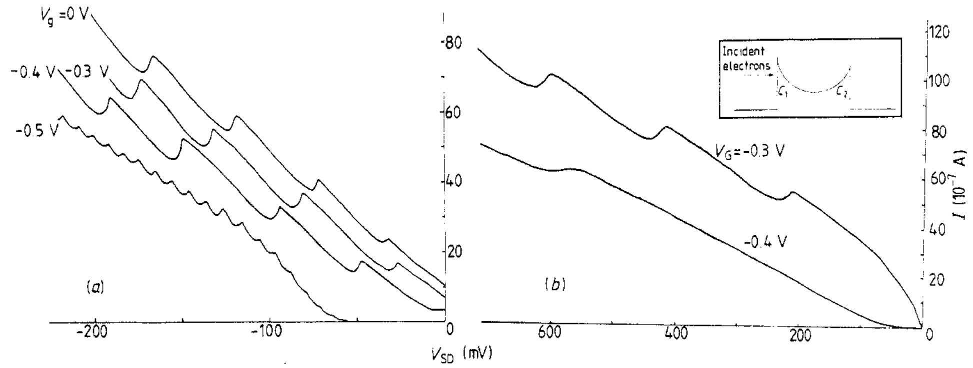


**Figure 2.** (*a*) The current–voltage characteristics at 4.2 K obtained from the DC-voltage-biased split gate device, with negative voltage bias, for $V_G = -0.5, -0.4, -0.3$ and 0 V, the characteristics are progressively displaced vertically by $2.5 \times 10^{-7}$ A. The high channel resistance for $V_G$ nominally zero indicates the initial narrow channel width. (*b*) With positive voltage bias, the sensitivity of the channel geometry to gate voltage is indicated by the large change in periodicity between $V_G = -0.3$ and $V_G = -0.4$ V, this latter value corresponding to the narrowest channel. The inset illustrates the potential experienced by the electrons for a small positive source–drain bias. The major effects are a rise in the conduction band edge minimum produced by a positive bias. To obtain conduction the positive drain bias has to be increased sufficiently for the minimum to line up with the Fermi energy.

parameters, the effect can be understood on the basis of electrostatics rather than the sequential transport of electrons. This would not, of course, apply to microwave properties of the device where an appropriate quantum treatment is required.

In order to discuss the results it is necessary to consider the potential distribution within the device in the pinched-off, high-source–drain-voltage regime. We suggest that the bending of the conduction band produces two capacitors in series as shown in the inset to figure 2(*b*), for both positive and negative source–drain voltages ($V_{SD}$). This situation is simple to visualise in the positive-bias situation; the conduction band edge will be higher in the 1D region compared with the 2D but will slope downwards towards the more positively biased end. However, due to the effect the positive source–drain bias has on the gate potential, the channel tends to close, thus raising the barrier to electronic transport and creating the two series capacitors with a potential minimum between them. In this case the presence of a positively charged impurity in the channel will enhance the potential well by which electrons tunnel in but its presence is not absolutely necessary to explain the effect. In the case of negative voltage on the drain the impurity is more necessary otherwise the potential well in the centre may not be strong enough to create two capacitors in series. In order to pass through the device, electrons must tunnel through both capacitances and charge can accumulate between them. The effect of $V_{SD}$ is to alter the channel geometry as well as applying an overall potential, and it is the role of channel geometry that is crucial in the experiment.

When nearly squeezed off the channel width is about $10^{-8}$ m and has length $\simeq 5 \times 10^{-7}$ m; the 'thickness' of the 2D electron gas is $\sim 10^{-8}$ m. These regions will act as the plates of a capacitor having a value of order $10^{-20}$ F but greater if the capacitor is shorter than the entire channel, i.e. in the range where single-electron effects will be observable. However, as the electron gas is depleted, it is more realistic to take the 'thickness' of the channel as more or less equal to the length. This gives a capacitance of

$\sim 10^{-18}$ F. As transport is ballistic, or quasi-ballistic, a typical electron transit time through the channel is $\sim 10^{-12}$ s. Such a time is comparable with, or less than, the mean emission time of electrons into the channel ($e/I$ where the current $I > 10^{-7}$ A); consequently the measurements are in the regime of current flow with more than one electron in the channel at a time, so allowing the possibility of space charge effects.

The current flowing through two, voltage-driven, small leaky capacitors (capacitance values $C_1$ and $C_2$ with corresponding values of resistance $R_1$ and $R_2$) in the single-electron transport regime has been analysed [7] using a classical treatment. It is found that the current increases in jumps of magnitude $e/R_2(C_1 + C_2)$, where electrons can tunnel rapidly through $R_1$ and space charge accumulates since $R_2 > R_1$ and provided $C_1 < C_2$. If these parameter requirements are not met then the steps are progressively washed out to yield a smooth characteristic. In general the voltages across the two capacitors $V_1$ and $V_2$ are given by

$$V_1 = \left(\frac{C_2}{C_1 + C_2}\right) V_T - \frac{ne}{C_1 + C_2} \qquad V_2 = \left(\frac{C_1}{C_1 + C_2}\right) V_T + \frac{ne}{C_1 + C_2}$$

where $V_T$ is the applied voltage and $n$ is the number of electrons trapped between the two capacitors. This treatment disregards the role of phase coherence which could produce a significant difference.

The essential difference between our system and that modelled elsewhere is that here the nature of the capacitances, and, hence, values of $C_1$, $C_2$, $R_1$ and $R_2$, are dependent on the value of the trapped charge. We suggest that an increase in the trapped charge by one electron alters the electrostatic potential and decreases the tunnelling probability. The net result is that the current falls rather than increases abruptly. Further increase in voltage increases the tunnelling probability in the normal way and also by altering the barrier height. In view of the general uncertainty of the parameters, $R_1$ could be of the same order as $R_2$. The most important aspect of the model is the effect of the trapped charge on the tunnelling process. The net result should be a superlinear increase in current between the drops. A crude estimate of the change in current is obtained by noting that [7] if $R_2 > R_1$ then

$$I = ne/R_2(C_1 + C_2).$$

Considering only the change in $R_2$ and assuming that $C_1$ and $C_2$ are relatively constant then the current falls if $1/n < \mathrm{d}R_2/R_2$ where $\mathrm{d}R_2$ is the increase in $R_2$. From the periodicity of the oscillations the value of $C_1 + C_2$ is in the region $10^{-17}$ to $10^{-19}$ F.

The results show that as a negative gate bias is increased so a larger $V_{SD}$ is required to turn on the conductance of the channel. This is illustrated in figure 2(*b*) for the gate voltages $V_G = -0.4$ V and $V_G = -0.5$ V where the channel is pinched off before the source–drain bias is applied. Greater voltages are required to turn the channel on, as the tunnelling probability for an electron is decreased when the barrier height is increased. Because of the need to induce tunnelling by a change of geometry the width of the zero-current region is not simply related to the capacitance as in the case considered previously in [7]. The main feature is the variation in the periodicity and magnitude of the oscillations with gate voltage. This is undoubtedly due to the potential profile seen by the incident electrons varying with the gate voltage.

The fact that oscillations are observed when the gate voltage is zero implies that a narrow channel is already present. In addition, the constancy of the periodicity also indicates that the channel geometry may be partially defined by an impurity. This effect has been sought in other lithographically identical devices with exactly the same experimental arrangement but has not been repeated, suggesting that this is a mesoscopic effect in the same category as conductance fluctuations due to impurities in small samples. We note that although 1D sub-bands will have formed, the number of oscillations found suggests that these are not the origin of the effect.

In conclusion, we have presented results indicating single-electron tunnelling events occurring within a one-dimensional channel created by a split-gate Schottky barrier on a GaAs/AlGaAs heterojunction. A classical model attributing these events to the formation of two effective capacitances in the channel has been discussed in which the geometry, and tunnelling probabilities, vary with the trapped charge. This model is thought appropriate in view of the phase-incoherent transport and general uncertainty of the device parameters. Finally we note that a recent model of conductance oscillations periodic in the gate voltage in narrow channels also utilises single-electron events and obtains good agreement with experiment [11, 12], indicating that these effects may be observed in a variety of small structures.

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